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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,042	12/29/2000	David I. Poisner	42390.P10586	9023

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EXAMINER	
VO, TIM T	

ART UNIT	PAPER NUMBER
2112	14

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/752,042	Applicant(s) POISNER ET AL.	
	Examiner Tim T. Vo	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

This application has been examined. Claims 1-12 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Gephardt et al. European patent application 0676686 A2 referred hereinafter "Gephardt in view of Klein patent number 6,029,223.

As for claims 1, 5 and 9, Gephardt teaches a method comprising:

asserting an edge-triggered interrupt signal from an input/output interrupt controller located within a system logic device to a local interrupt controller within a processor (see figure 2, system 200 discloses peripheral device 204 from external bus 206 generate interrupts to the PM MESSAGE UNIT 232, wherein the PM MESSAGE comprises interrupt detector 306 also the interrupt detector 306 coupled to the interrupt controller 224 and page 4 lines 51-58, wherein peripheral devices 204 send request on bus 206 to the integrated processor 202 via bus interface 228); and

delivering an interrupt pending signal from the processor to a power management unit located within the system logic device (see figure 2, system 200

discloses integrated processor 202, power management unit 208 and PM message bus 210 and page 5 lines 6-41, wherein the integrated processor receives request detects from the bus request detector 302. The integrated processor then generates PM messages to the power management unit 260, wherein the PM messages comprises all of the messages in table I which included a timer interrupt is pending or in service).

Gephardt does not expressly teach wherein the local interrupt controller is located within a processor. However, this feature is well known as Klein discloses in figure 2, wherein the local interrupt controller 46 is located within the CPU 46 (see column 6 lines 4 lines 52-67 of Klein). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Klein to the teachings of Gephardt because there are many advantages are achieved by integrating local interrupt controller into the processor to reduce number of pins and signal lines complexity (see column 6 lines 43-60 of Klein).

2. As for claims 2, 6 and 10, Gephardt teaches the power management device causing the processor to enter a high power state if the processor is in a low power state when the processor delivers the interrupt pending signal to the power management device (see figure 5, state 502, state 504, and figure 6, state 602, 604, 606 revert back to ready state 600 and page 5 lines 48-57 and page 6 lines 46-54, wherein figure 5 discloses the integrated processor 202 is in idle mode 502 and activity detected 504 when there is an interrupt, thus figure 6 discloses the integrated processor 202 is dynamically switching from ready state 600 (high power state) to suspend state

606 (low power state) and vice versa from (suspend state (low power state) ready state 600 (high power state).

3. As for claims 3, 7, and 11, Gephardt teaches wherein delivering an interrupt pending signal includes delivering the interrupt signal from the processor to the power management device over a signal line coupled between a single processor pin and the power management device (see figure 2, integrated processor 202, PM message 210, power management state machine 260 and page 5 lines 6-41, wherein the integrated processor receives request detects from the bus request detector 302. The integrated processor then generates PM messages to the power management unit 260, wherein the PM messages comprises all of the messages in table I which included a timer interrupt is pending or in service).

4. As for claims 4, 8, 12, Gephardt teaches wherein causing the processor to enter a high power state includes the power management device deasserting a stop clock signal (see figure 7, power management state machine 260, clock control unit 264, stop CPU signal line, 202, wherein the power management sent a control stop signal to the integrated processor 202).

Response to Arguments

In response to the applicant's arguments that Gephardt does not teach an input/output interrupt controller located within a system logic device. Examiner refers the system 200 in figure 2 as a system logic device thus, the interrupt controller is located within the system 200. This teaching is equivalent to the breadth of the claim.

In response to the applicant's arguments that Gephardt does not teach the local interrupt controller located within a processor, see claim 1 rejection above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim T. Vo whose telephone number is 703-308-5862. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tim T. Vo
Primary Examiner
Art Unit 2112

4/18/04